REMARKS

Claims 1-27 are all the claims pending in the application. Claims 1-27 stand rejected on prior art grounds. Applicants respectfully traverse this rejection based on the following discussion.

I. The Prior Art Rejections

Claims 1-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Manufacturing, hereinafter "Manufacturing" in view of Evans et al., hereinafter "Evans" (6,775,647). Applicants respectfully traverse this rejection based on the following discussion.

A. Lack of Prima Facie Case of Obviousness

In response to Applicant's argument that the references are from non-analogous art fields and are not properly combinable, the Examiner asserts that Evans et al. is "reasonably pertinent to the particular problem in manufacturing with which the applicant is concerned."

Assuming the Examiner is correct in considering the art cited as analogous, it still remains that the Examiner has failed to establish her *prima facie* case of obviousness for at least two reasons. First, the combination of Meieran et al. 21st Century Semiconductor Manufacturing Capabilities Intel Technology Journal Q4 1998 pp1-8 ("Manufacturing") and US Patent Number 6,775,647 B1 ("Evans") fails to disclose each and every limitation of the claimed invention. Second, the Examiner has failed to provide adequate motivation for combining the teachings of Manufacturing and Evans.

1. **Manufacturing and Evans fail to disclose each and every limitation of the claims.**

The proposed combination of Manufacturing and Evans fails to teach each and every element of the claimed invention. Specifically, the Examiner even acknowledges that Manufacturing fails to disclose a regression analysis on historical costs of historical critical gate dimensions at a specific fabricator and then uses the historical critical gate dimensions as independent variables and the historical costs as dependent variables in order to produce models as recited in the claims.

The Manufacturing reference is extremely general and, other than describing various noble goals relating to chip complexity, cost per chip element set, yield percentage, etc., the Manufacturing reference is silent as to how such goals could be achieved. Manufacturing fails to disclose critical gate dimensions such as the size and thickness of the source and drain regions, the size and depth of the channel region, the size and thickness of the gate oxide, sizes and positions of spacers adjacent the gate, sizes and dimensions of various contacts and insulators connected to the source, and drain, and gain regions. Indeed, the Examiner states that Manufacturing does not expressly disclose performing a regression analysis on historical costs of historical critical gate dimensions. Therefore, the bulk of the teaching of the narrowly claimed system and method would have to be found in the Evans reference if the rejection were to be meritorious.

The claims define that the models only show the relationship between the historical critical gate dimensions and historical costs. For example, independent claims 1, 8, and 21 "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" (this is similarly defined by independent claim 15). This limitation is not disclosed in either Manufacturing or Evans. Thus, the claims are narrowly limited to predicting semiconductor product costs from historical critical gate dimensions. There simply is no corresponding teaching in the prior art of record for such claimed features.

The Examiner cites Evans to cure the deficiency of Manufacturing acknowledged by the

Examiner and referred to above. However, Evans also fails to disclose a regression analysis on historical costs of historical critical gate dimensions at a specific fabricator and then uses the historical critical gate dimensions as independent variables and the historical costs as dependent variables in order to produce models as recited in the claims.

Even if one were to ignore the fact that Evans relates to aircraft parts and thus provides no motivation to combine its disclosure with Manufacturing, Evans discloses predicting cost based on actual dimensions of materials of a finished piece in an aircraft not the historical dimensions and historical costs. To the contrary, Evans requires that the dimensions of each part needs to be specified in the regression analysis (see column 2, lines 19-34 and column 5, lines 19-39 of Evans). If Evans' teaching were translated into semiconductor manufacturing processes, Evans would require that the size and dimensions of the gate, gate oxide, source, drain, channel, contacts, etc. all be specified in order to arrive at a future cost prediction for the completed product (e.g., a transistor). Therefore, even if the teachings of Evans were applied to semiconductor manufacturing processes, Evans still would not teach or suggest to one ordinarily skilled in the art a system and method for predicting costs of semiconductor products based only on the critical gate dimension (as claimed).

Moreover, because Evans is rooted in the technology of manufacturing aircraft engines, it does not discuss the relationship between historical critical gate dimensions and historical costs (nor would it be expected to). There simply is no teaching for the claimed invention which provides the benefit of allowing the user to input only the gate dimensions to achieve a prediction of future costs for entire semiconductor products. There are many different dimensions within semiconductor devices such as the size and thickness of the source and drain regions, the size and depth of the channel region, the size and thickness of the gate oxide, sizes and positions of spacers adjacent the gate, sizes and dimensions of various contacts and insulators connected to the source, and drain, and gain regions.

The claimed invention is able to predict the product costs of new semiconductor devices (e.g., whole transistors) simply by specifying a new gate dimension, without having to specify dimensions, sizes, locations, thickness of any other elements such as source, drain, gate oxide,

contacts, channel region, etc. To equate the claimed ability to predict costs into an aircraft engine industry manufacturing process would require a teaching of predicting the cost an airplane based on the size of a given bolt or nut. Evans clearly does not provide such teaching.

Additionally, Applicants note that even if one ordinarily skilled in the semiconductor product cost estimating field had made reference to Evans, the proposed combination of references still would not teach or suggest that the regression analysis should be limited only to historical critical gate dimensions as is required by independent claims 8, 15, and 21. As shown in the previous discussion, the Manufacturing reference does not discuss calculating future costs based upon historical critical gate dimensions. Instead, the Manufacturing reference only makes forecasts of chip complexity, cost per chip element set, yield percentage, etc. Evans only discusses the manufacturing of aircraft engines and is completely silent regarding any aspects of semiconductor manufacturing. Therefore, Evans also omits any teaching of limiting the regression analysis to critical gate dimensions.

Therefore, it is Applicants' position that the Manufacturing paper, even if combined with Evans, does not teach or suggest the claimed ability to "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" as defined by independent claims 1, 8, and 21 (and similarly defined by independent claim 15).

Thus, Applicants submit that independent claims 1, 8, 15, and 21 are patentable over the proposed combination of the Manufacturing paper and Evans. Further, dependent claims 2-7, 9-14, 16-20, and 22-27 are similarly patentable, not only because they depend from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

2. Lack of Motivation to Combine Manufacturing and Evans

The Office Action notes that Manufacturing does not expressly disclose performing a regression analysis on historical costs of historical critical gate dimensions. To cure this

deficiency, the Office Action refers to Evans for teaching a method of estimating manufacturing costs using a regression analysis. However, Evans relates to estimating costs within the field of aircraft engines (column 1, lines 32-37; column 5, lines 40-50) while all independent claims are specifically limited to performing "a regression analysis on historical costs of historical critical gate dimensions" for "semiconductor product costs."

The Examiner argues that the teachings from these somewhat diverse technical fields (aircraft engines and semiconductors) would have been combined by one ordinarily skilled in the field of predicting costs for developing new products.

Presumably the Examiner is proposing that an individual interested in optimizing a manufacturing process would be motivated to look across many different technologies when developing manufacturing techniques. While this argument initially appears attractive (or at least plausible), it ignores the specific nature of "gate dimensions" within "semiconductor product costs" which are unique to the semiconductor manufacturing industry and which would not benefit from teachings within different technologies, such as the aircraft engine technology of Evans. There are many different dimensions within semiconductor devices such as the size and thickness of the source and drain regions, the size and depth of the channel region, the size and thickness of the gate oxide, sizes and positions spacers adjacent the gate, sizes and dimensions of various insulators and contacts connected to the source, drain, and gain regions.

The claimed invention is able to predict the product costs of new semiconductor devices simply by specifying a new gate dimension, without having to specify dimensions, sizes, locations or thicknesses as of any other elements such as source, drain, gate oxide, contacts, channel region, etc. in other words, the claimed invention is very specifically related to semiconductor devices and omits the need to provide dimensions of all elements of the semiconductor device when predicting future costs. To the contrary, because Evans is rooted in aircraft engine technology, and not semiconductor technology, Evans requires the sizes, dimensions, etc. of future products to be specified when making costs predictions. Therefore, one skilled in the art of optimizing semiconductor manufacturing processes would not have made reference to aircraft engine manufacturing processes when attempting to develop a system of

predicting costs of semiconductor products by supplying the dimension of a single component within the device.

Therefore, one of ordinary skill in the art would not have been motivated to combine the teachings from Manufacturing and Evans because Evans discloses predicting cost based on actual dimensions of materials of a finished piece in an aircraft not the historical dimensions and historical costs. Even if one were to ignore the fact that Evans relates to aircraft parts and thus provides no motivation to combine its disclosure with Manufacturing, the approach disclosed in Evans requires specific knowledge of the actual dimensions of the finished piece to predict cost rather than a backward looking analysis of historical data to predict future cost of semiconductor products.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-27, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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